EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John Serio on 11/9/09.

The application has been amended as follows:

Claim 15, line 1: Insert "computer implemented" before "process".

The following is an examiner's statement of reasons for allowance:

The closest prior art (e.g. "Determining the Optimum Extended Instruction-Set Architecture for Application Specific Reconfigurable VLIW CPUs" by Alippi et. al) discloses generating a micro-processor instruction set extension for a processor application, comprising:

generating a data flow graph G(V,E) of nodes V representing primitive operations of the processor application and edges E representing data dependencies of said application (pg. 51, col. 2, 1st par. in section 3 "translated into ... a Data Flow Graph");

evaluating subgraphs S of G(V,E) as candidates for an instruction set extension, each said subgraph S having a number of inputs IN(S) and a number of outputs

OUT(S), said instruction set extension having a number of available register-file read ports Nin and a number of available register-file write ports Nout; and

transforming said instruction set by adding an instruction set extension representing an identified candidate to said instruction set.

The closest prior art does not disclose or suggest evaluating a subgraph S includes:

if OUT(S) is less than or equal to Nout, and

if S is convex, wherein S is convex when no path exists from a node in S to another node in S when said path involves a node that is not in S, and

if IN(S) is less than or equal to Nin,

then identifying S as a candidate for transformation into an instruction set extension, else disregarding S as a candidate for transformation into an instruction set extension;

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON MITCHELL whose telephone number is (571)272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bullock Lewis can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason Mitchell/
Primary Examiner, Art Unit 2193